REMARKS

Claims 1-4, 6-8, 11-13, 15-21 and 23 are pending. No claims are amended herein. The Applicant respectfully requests reconsideration of the Claims in light of the discussion set forth below.

112 Rejection

Claims 1-4, 6-8, 11-13, 15-21 and 23 are rejected under 35 U.S. C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Examiner has misunderstood the claims to include the word "immediate" instead of "intermediate." The Applicant respectfully submits that this misunderstanding is the source of the Examiners objections to Claim 1. As the recitation in the claims is indeed "intermediate" and not "immediate" the Applicant respectfully requests the withdrawal of the 112 second rejection of Claims 1-4, 6-8, 11-13, 15-21 and 23.

35 U.S.C. §103

Claims 1-4, 6-8, 11-13, 15-21 and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kadanka et al. (U.S. Patent No. 5,621,308) in view of newly cited art to Mietus (U.S. Patent No. 5,666,046). Applicants have reviewed the recited references and respectfully submit that the present invention, as is recited in Claims 1-4, 6-8, 11-13, 15-21 and 23, is neither anticipated nor rendered obvious by Kadanka and Mietus, either alone or in combination.

The Examiner's attention is respectfully directed to independent Claim 1 which recites that an embodiment of the Applicant's invention includes a band-gap reference circuit, comprising:

> ...a band-gap reference unit; buffer circuit electronically coupled with said band-gap reference unit; and a voltage pull-up device electronically coupled between and located intermediate to said band-gap reference unit and said buffer circuit, wherein said voltage pull-up device acts to reduce a required supply voltage to maintain a band-gap reference

voltage and wherein said voltage pull-up device is implemented as a transistor with a VBE of less than 1.0 volts.

Claims 7 and 16 contain limitations similar to those contained in Claim 1. Claims 2-4, and 6 depend from claim 1 and recite further features of the claimed invention. Claims 8, 11-13 and 15 depend from claim 7 and recite further features of the claimed invention. Claims 15-21 and 23 depend from claim 7 and recite further features of the claimed invention.

Kadanka et al. does not anticipate or render obvious a band-gap reference circuit that includes "a voltage pull-up device electronically coupled between and located intermediate to said band-gap reference unit and said buffer circuit, wherein said voltage pull-up device acts to reduce a required supply voltage to maintain a band-gap reference voltage and wherein said voltage pull-up device is implemented as a transistor with a VBE of less than 1.0 volts" as is recited in the Claims. In order to meet the limitations of Claim 1 (Claims 7 and 16 contain similar limitations) a reference must show or suggest either expressly or inherently, at the very least the basic components of the claimed invention such as: (1) a voltage pull-up device, (2) a band-gap reference unit and (3) a buffer circuit.

Kadanka et al. only shows an electrical apparatus for providing a reference signal that includes a regulator portion that provides a substantially constant current. It is important to note that Kadanka et al. simply does not discuss a buffer circuit or a voltage pull-up device. In fact, Kadanka et al. discloses that element 54, cited in the Office Action as being equivalent to the recited buffer circuit is actually a part of "voltage reference circuit 39." Moreover, Kadanka et al discloses that element 70, cited in the Office Action as being equivalent to the recited voltage pull-up device is actually the "regulator portion" of voltage reference circuit 39. However, these

interpretations of the claim limitations are at odds with Applicant's specification which simply does not disclose that the recited buffer be equivalent to a regulator. The Examiner is respectfully reminded that claim limitations must be interpreted in light of Applicant's specification and cannot be interpreted in a manner that contradicts the Applicant's specification.

In fact, nowhere in the Kadanka et al. reference is a voltage pull-up device that is electronically coupled between and located intermediate to said band-gap reference unit and said buffer circuit, wherein the voltage pull-up device acts to reduce a required supply voltage to maintain a band-gap reference voltage and wherein the voltage pull-up device is implemented as a transistor with a V_{BE} of less than 1.0 volts as set forth in Claim 1 and disclosed in the Applicant's specification shown or suggested. Consequently, the embodiments of the Applicant's invention as are set forth in Claims 1, 7 and 16 are neither anticipated nor rendered obvious by Kadanka et al.

Mietus does not teach or suggest a modification of Kadanka et al. that would remedy the deficiencies of Kadanka et al. outlined above. More specifically, Mietus does not teach or suggest a band-gap reference circuit that includes "a voltage pull-up device electronically coupled between and located intermediate to said band-gap reference unit and said buffer circuit, wherein said voltage pull-up device acts to reduce a required supply voltage to maintain a band-gap reference voltage and wherein said voltage pull-up device is implemented as a transistor with a V_{BE} of less than 1.0 volts" as is recited in the Claims. In fact, nowhere in the Mietus reference is a voltage pull-up device that is electronically coupled between and located intermediate to said band-gap reference unit and said buffer circuit, wherein the voltage pull-up device acts to reduce a required supply voltage to maintain a band-gap reference voltage and wherein the voltage pull-

up device is implemented as a transistor with a V_{BE} of less than 1.0 volts as set forth in Claim 1. Consequently, the embodiments of the Applicant's invention as are set forth in Claims 1, 7 and 16 are neither anticipated nor rendered obvious by Kadanka et al. in view of Mietus.

Therefore, Applicant respectfully submit that Kadanka et al. in view of Mietus does not anticipate or render obvious the present claimed invention as recited in Claims 1, 7, and 16 and, as such, Claims 1, 7, and 16 overcomes the basis for rejection under 35 U.S.C. § 103. Accordingly, Applicants respectfully submit that Claims 1, 7, and 16 are in condition for allowance. In addition, Applicants respectfully submit that Kadanka et al. in view of Mietus does not anticipate or render obvious the present invention as is recited in Claims 2-4 and 6 which depend from independent Claim 1, Claims 8, 11-13 and 15 which depend from independent Claim 7, and Claims 15-21 and 23 which depend from independent Claim 16, and that Claims 2-4, 6, 8, 11-13, 15-21 and 23 are also in condition for allowance as being dependent on an allowable base claim.

CONCLUSION

In light of the foregoing amendments and remarks, Applicant respectfully submits that the remaining claims are in condition for allowance. Applicant respectfully requests allowance of the pending Claims.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

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Respectfully submitted,

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